JUNXUAN LIAO

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EDUCATION

School of Computer Science, Wuhan University *2020 - 2024(expected)*

Undergraduate in Computer Science. GPA: 3.94/4 TOEFL: 114

GRE: Q 170, V 167, AWA 4

EXPERIENCE

Teaching Assistant, Wuhan University *2021 - 2023*

- Worked as a teaching assistant for two key courses: *Introduction to Computer Systems* and *Computer Organization and Design*.
- Instructed on the labs of *Computer Systems: A Programmer's Perspective*. Rewrote and fixed some of them.
- Gave a presentation for a livestream organized by the Chinese publisher of *CS: APP*.

RESEARCH PROJECTS

A Linux-capable MIPS Processor [Code]

- Implemented a fully-functional MIPS processor with parameterized caches in ~7000 lines of Verilog.
- Constructed an SoC on FPGA and ported the Linux kernel.
- Gained extensive experience in debugging FPGA designs, Linux Kernel and U-Boot the bootloader.
- Fixed an ethernet driver bug in U-Boot and sent a patch.

Introduction to the Linux Kernel [PDF(in Chinese)]

- Wrote a 52-page case study on the Linux kernel.
- Researched the design of the Linux kernel by reading its source code and documentation.
- Analyzed the design and implementation of process management, memory management, file system, etc of the Linux kernel.

Container Scheduling in Serverless Computing
Advisor: Yili Gong, Chuang Hu (Wuhan University)

- Analyzed and improved existing caching-based container keep-alive policies.
- Proposed a new container scheduler that optimizes the allocation of memory among user functions to reduce the number of cold starts and improve the throughput.
- Implemented the scheduler in OpenWhisk, a real-world serverless platform, and evaluated its performance against state-of-the-art methods.
- Submitted the manuscript to EuroSys 2024 for review as the first author.

A Scalable Simulator for CXL-based Shared Memory Clusters (Ongoing)
Advisor: Yili Gong, Chuang Hu (Wuhan University)

- Leading the design and implementation of the simulator, aiming to provide an evaluation platform for next-generation computer clusters with CXL-enabled shared memory.

- Leveraging dynamic binary translation and distributed parallel discrete event simulation to model performance and achieve transparent memory sharing.
- Implementing distributed modeling of out-of-order cores, cache-coherent CXL memory systems, on-chip networks, etc. to provide scalable and accurate simulation.

SKILLS

Programming Languages: Rust, C, Python, Verilog, C++, Haskell, Assembly